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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,435	06/07/2000	Haruko Aoyama	P/2371-32	1097

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EXAMINER

BADERMAN, SCOTT T

ART UNIT PAPER NUMBER

2113

DATE MAILED: 04/19/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

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## Office Action Summary

Application No.

09/589,435

Applicant(s)

AOYAMA, HARUKO

Examiner

Scott T Baderman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-4 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 07 June 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Tamura (European Patent Application 0 640 916 A2).

As in claim 1, Tamura discloses a computer system comprising a CPU for operating with pipeline processing (Figure 1, element 13), a ROM storing a program to be executed by the CPU (Figure 1, element 3, column 8: lines 14-15), and at least one ROM correction unit (being that the program being corrected is stored in the ROM) including a first storage unit for storing a subject address (i.e., the bug address) of an original instruction group in the program having a bug therein (Figure 2, column 8: line 55 – column 9: line 8), a second storage unit for storing a modified instruction group for replacing the original instruction group by the modified instruction group having a branch address (Figures 1, 2 and 4, column 8: lines 8-12, column 9: lines 2-15, column 10: line 26 – column 11: line 28), a comparator for comparing a current address of a current instruction read from the ROM against the subject address (Figure 1, column 7: lines 25-34), a selector for selecting the current address or the branch address based on a result

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of the comparison by the comparator (Figure 1, column 7: lines 34-46), and a flag generator for setting a ROM correction flag when the selector selects the branch address, wherein the flag is outputted through a data bus (i.e., the flag is outputted under the control of the instruction executing unit, wherein since the instruction executing unit outputs data (signals) across a bus (e.g., the bus between the instruction executing unit and the selector in Figure 6), the flag is also outputted across the bus) (Figures 6 and 7, column 12: lines 3-31).

As in claim 2, Tamura discloses a plurality of ROM correction units (Figure 8, column 13: line 33 - column 14: line 10).

As in claim 3, Tamura discloses wherein the flag is set at an execution stage of a branch instruction indicating the current address to jump to the branch address (column 12: lines 3-31).

As in claim 4, Tamura discloses that the modified instruction group is supplied from outside the computer system (Figure 1, element 14, and Figure 4, column 8: lines 8-12 and 47-55).

### ***Response to Arguments***

Regarding claim 1, the Applicant argues that as result of the claimed structure, the CPU can judge the operation of the ROM correction unit based on the ROM correction flag delivered through a data bus, however, the claim only mentions the delivery of the correction flag through a data bus. This language reads broadly and is still anticipated by Tamura (European Patent

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Application 0 640 916 A2). The Applicant is directed to the rejection above for the reasoning of the rejection.

***Conclusion***

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Scott T Baderman  
Primary Examiner  
Art Unit 2113

STB